Doc Code: AP.PRE.REQ

PTO/SB/33 (07/05)
Approved for use through xx/xx/200x. OMB 0651-00xx
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
890A.0001.U1(US)

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on September 5, 2006

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Application Number	Filed
10/691,252	10/22/2005

First Named Inventor
Michael Buchmann

Art Unit	Examiner
2838	Bao Q. Vu

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [x] attorney or agent of record. Registration number 41,180
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

Signature

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September 5, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of _ forms are submitted.

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of:

APPLICANT: Michael Buchmann

SERIAL NO.: 10/691,252	FILING DATE:	October 22, 2003
EXAMINER: Bao Q. Vu	ART UNIT:	2838
ATTORNEY'S DOCKET NO.:	890A.0001.U1(US)	

TITLE: Voltage Multiplier with Charge Recovery

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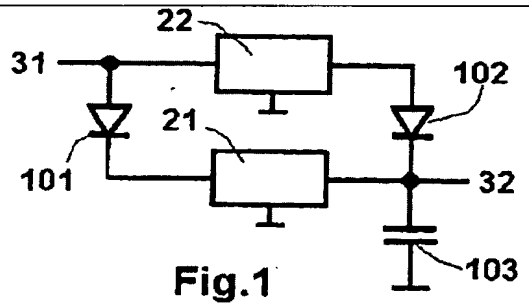
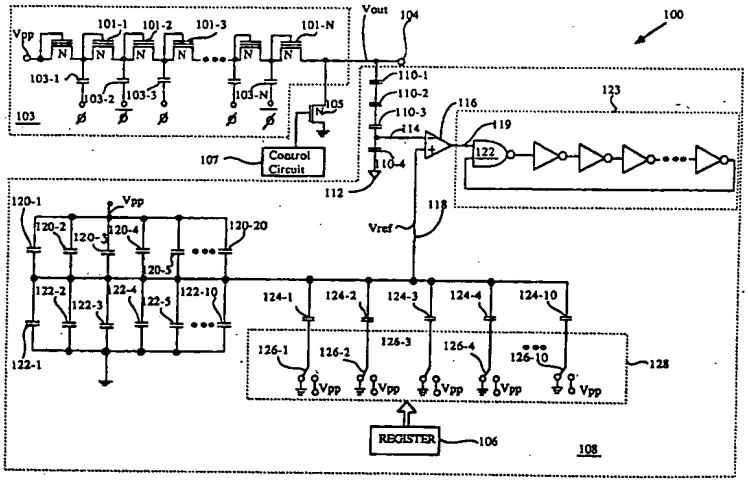
PRE-APPEAL BRIEF REQUEST FOR REVIEW ATTACHMENT

The following is a concise recitation of a clear error in the Examiner's rejections regarding this application.

The present application contains claims 1-8, of which claim 1 is the sole independent claim. A portion of independent claim 1 is shown on the left side of the following table. On the right side, a portion of FIG. 1 of the present application is shown for ease of reference. FIG. 11 shows examples of elements 21 and 22 in greater detail.

Capacitive voltage multiplier ..., wherein the multiplier comprises a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier, said switching capacitor circuit (21) provided with capacitors and switches for charging the capacitors in parallel and discharging them in series in order to deliver a high voltage pulse, characterised in that the multiplier further comprises a diode chain circuit (22) coupled between said input (31) and output (32) terminals of the multiplier, said diode chain circuit (22) comprising a diode-chain and pumping capacitors for delivering high voltage current.	 Fig.1

The Examiner rejects all claims based on a combination of Kazerounian, U.S. Patent No. 5,006,974, and Yu, U.S. Patent No. 6,304,007. In particular, the Examiner asserts "Kazerounian discloses a capacitive multiplier circuit having a diode chain (103) and a charge pump circuitry (128) that [is] connected between the input and output of the multiplier circuit (100)." The Examiner appears to assert that block 103 meets the subject matter of "a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier" in independent claim 1. The Examiner cites and displays FIG. 2 from Kazerounian, reproduced below:



Before proceeding further with an argument, it is helpful to review Kazerounian. The following description in this paragraph is from Kazerounian, col. 8, lines 9-38. The capacitors 110-1 through 110-4 act as a voltage divider. Comparator 116 compares V_{OUT} and V_{REF} and produces a signal 119 for input into ring oscillator circuit 124 (incorrectly marked as 123 in FIG. 2). When V_{OUT} is not equal to V_{REF}, ring oscillator circuit 124 generates "clock signals ϕ and $\overline{\phi}$, and thus voltage multiplier 100 will increase voltage V_{OUT} at lead 104. However, as soon as voltage $V_{OUT}/4$ is greater than voltage V_{REF}, the signal at output lead 119 goes low, ring oscillator 124 stops oscillating and voltage multiplier 100 stops increasing voltage V_{OUT}. Thus, the EEPROM of the present invention includes a voltage regulator which permits voltage V_{OUT} to be accurately controlled." Kazerounian, col. 8, lines 30-38. The clock signals ϕ and $\overline{\phi}$ are inputs into block 103 (note that capacitors 103-1 to 103-N are also marked as "103"). The output of voltage multiplier 100 is the output lead 104, which carries V_{OUT}. The "input" to block 103 is V_{PP}.

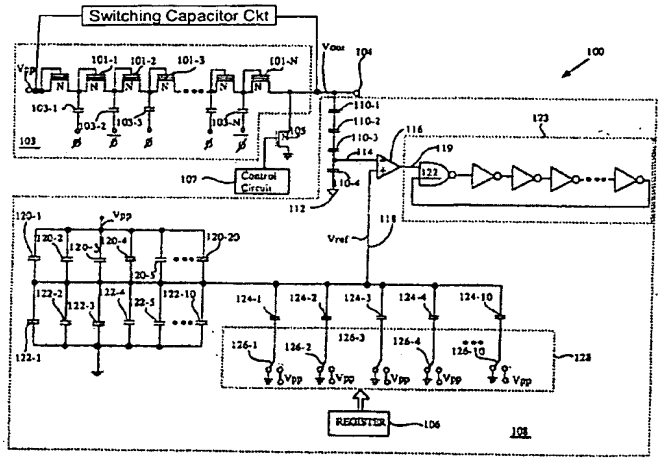
Furthermore, the circuitry in Kazerounian is specifically designed so that one can select the ***lowest*** Vout 104 that erases an EEPROM. The selection is performed using the register 106 and a particular process. See the text from col. 8, line 52 to col. 9, line 38 of Kazerounian. In particular, Kazerounian states the following:

> This process continues until a voltage is selected which is sufficient for erasing the EEPROM. Thereafter, the contents of nonvolatile register 106 are no longer changed, and the EEPROM is erased with the selected voltage. By limiting voltage V_{OUT} to a voltage large enough to erase the EEPROM but not greater, the transistors exposed to voltage V_{OUT} will not be excessively stressed.

Kazerounian, col. 9, lines 31-38.

Based on the cited sections of Kazerounian, Applicant reads Kazerounian as providing a voltage multiplier circuit 100 that allows selection of a reference voltage, V_{REF}, based on contents of a register. Kazerounian discloses a voltage multiplier circuit 100 that is ***carefully designed*** to allow selection of the lowest V_{OUT} that will allow an EEPROM to be erased.

Into this carefully designed system, the Examiner asserts that a multiplier/charge pump having capacitors charged in parallel and discharged in series should be added. The Examiner cites Yu, col. 1, lines 18-22 for disclosure of a "switching capacitor circuit". In order for the switching capacitor circuit of Yu to be added into the invention in Kazerounian and meet the subject matter of independent claim 1, the following would have to occur (as illustrated by a modified version of FIG. 2 of Kazerounian):



This is true because the Examiner appears to assert that element "103" meets the subject matter of "diode chain circuit (22) coupled between said input (31) and output (32) terminals of the multiplier". Assuming, *arguendo*, the Examiner's assertion is true, V_{PP} is the input of block 103 and V_{OUT} (e.g., output lead 104) is the output for both block 103 and multiplier circuit 100. Then in order for the switching capacitor circuit of Yu to meet the subject matter of "a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier" in independent claim 1, the switching capacitor circuit would be placed between V_{PP} and V_{OUT}, as shown above in the modified FIG. 2 of Kazerounian.

For at least the following reasons, the combination of Kazerounian and Yu is improper and the requirements of a *prima facie* case of obviousness are not met:

First, the circuitry of Kazerounian already produces a high output voltage on V_{OUT} 10 (see FIG. 2 of Kazerounian). There is no benefit to adding yet another circuit (i.e., from Yu) for producing a high voltage on V_{OUT} 104 of Kazerounian.

Second, combining two circuits (block 103 in Kazerounian and the circuit described at col. 1, lines 18-22 of Yu, as shown above in modified FIG. 2 of Kazerounian), each of which produces a high voltage from a lower input voltage, would appear to provide no benefits and many detriments to Kazerounian. The circuitry in Kazerounian is specifically designed so that one can select the ***lowest*** V_{OUT} 104 that erases an EEPROM. The selection is performed using the register 106 and a particular process. See the text from col. 8, line 52 to col. 9, line 38 of Kazerounian. Adding another circuit that produces an even higher voltage at V_{OUT} 104 would be counterproductive and may render impossible the careful selection of V_{OUT} 104. For instance, V_{OUT} 104 in such a combined system would now depend on two circuits for producing a high voltage output instead of basically a single circuit (block 103) in Kazerounian. Furthermore, the Yu circuit does not appear to have an adjustable voltage and does not appear to be able to be controlled by elements (e.g., capacitors 110, the ring oscillator circuit 124, the circuits adjusting V_{REF}, and the comparator 116) in Kazerounian that select a voltage on V_{OUT} 104. Therefore, the combination of Kazerounian and Yu may not provide adjustable V_{OUT}, which is one of the primary reasons Kazerounian was invented.

Third, the effect of adding the switching capacitor circuit in parallel with block 103 in Kazerounian is unclear. For instance, if the switching capacitor circuit produced V_A

and block 103 produces V_B, what would V_{OUT} be? Would V_{OUT} be the addition of V_A and V_B, the subtraction of V_A and V_B, or some other possibility? The Examiner has given no explanation of how adding the switching capacitor circuit in parallel with block 103 in Kazerounian would operate, and therefore a *prima facie* case of obviousness is not shown.

Finally, Kazerounian teaches away from a combination of Kazerounian and Yu at, e.g., col. 2, lines 8-19, where Kazerounian states that prior art regulating circuits were too much dependent on manufacturing processes. Adding, as the Examiner suggests, a switching capacitor circuit into the system of Kazerounian, where the switching capacitor circuit is not subjected to the voltage regulation of multiplier circuit 100 of Kazerounian, would create the same problem that the invention of Kazerounian was trying to fix.

For at least these reasons, the combination of Kazerounian and Yu is improper and the requirements of a *prima facie* case of obviousness are not met. Independent claim 1 is therefore patentable, as are claims 2-8, which depend from claim 1.

Furthermore, the circuit in FIG. 1 (and as claimed in the claims) is a model of simple functionality for its purpose, whereas the Kazerounian circuit is a complex circuit for another purpose with arrangements for achieving that other purpose. Moreover, Kazerounian is completely lacking the non-obvious rectifying functions provided by element 101 (dependent claim 8) and element 102 (dependent claim 7) in FIG. 1 that are important to charge preservation, a concept which is not even discussed in or implied by Kazerounian or Yu or their combination. Therefore, claims 7 and 8 (for example) present subject matter not made obvious by the references of record.

Respectfully submitted:

9/5/06

Robert J. Mauri, 41,180 — Date

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